

## Design and Optimisation of Circular and Inductors for Silicon-based RFIC Application

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### 1. Introduction

In this paper, spiral inductors for RF application, which are designed on a silicon substrate by using standards  $0.35\ \mu\text{m}$  CMOS technology, are described. Analyzed and designed with ASITIC (a tool from the University of Berkeley), which accurately takes into account the parasitic effects. This study shows the possibility of obtaining an optimal inductance having a high quality factor of 15. This result is carried out without resorting to the specific processes such as the digging of the substrate under the inductors or the use of a thick layer in gold. The use of circular form, with optimization of geometrical parameters like spacing between two adjacent turn, the track width and the number of turns, can ensure high quality factors.

### 2. Results

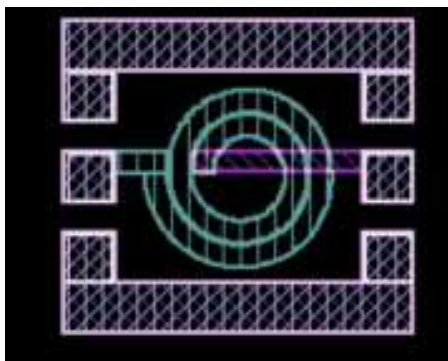


Fig.1: Design of circular inductor 2-turn,  $2\ \mu\text{m}$  spacing and width  $45\ \mu\text{m}$ .

#### a) Effects of metal conductor width

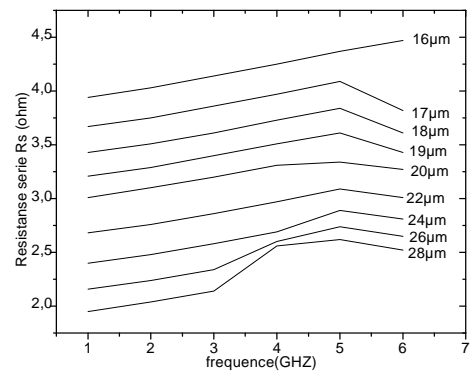


Fig.2: Inductance versus frequency for 2-turn and  $2\ \mu\text{m}$  spacing with width varying from  $16\ \mu\text{m}$  to  $28\ \mu\text{m}$ .

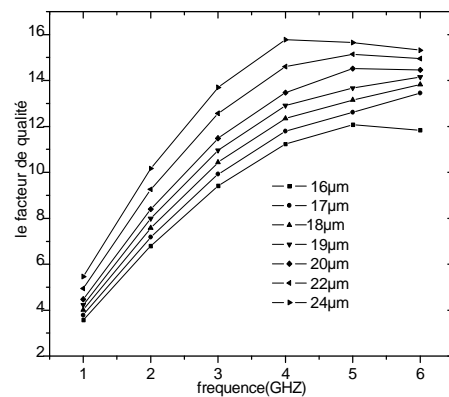


Fig.3: Quality factor versus frequency for 2-turn and  $2\ \mu\text{m}$  spacing with width varying from  $16\ \mu\text{m}$  to  $28\ \mu\text{m}$ .

b) *Effects of metal conductor-to conductor spacing*

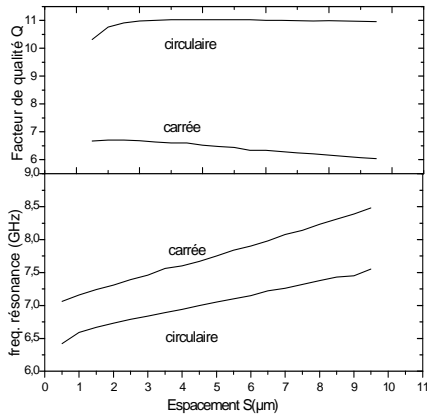


Fig.4: Quality factor and frequency of resonance for 3-turn and 25µm width with spacing varying from 0.5µm to 10µm.

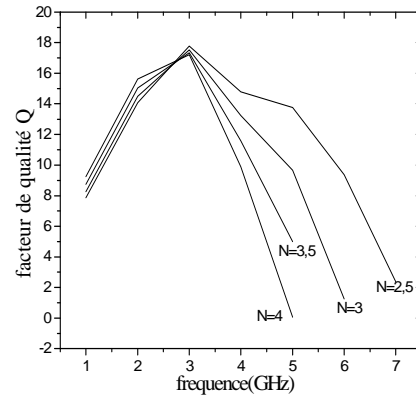


Fig.6: Quality factor versus frequency for 25µm width and 2µm spacing with number of turn varying from 1 to 4.

c) *Effects of number of turns*

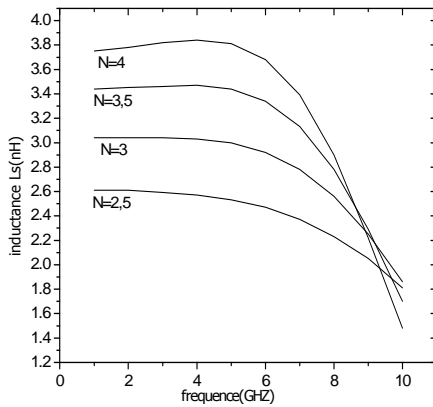


Fig.5: Inductance versus frequency for 25µm width and 2µm spacing with number of turn varying from 1 to 4.